between selected metals. A technique for fabricating a MSM heterojunction diode is described in detail below.

[0027] 1. Shallow Contact Doping.

[0028] Depending on the application of the MSM diode, the surface of one or both sides of the silicon layer **401** can be doped for creation of an ohmic contact for carrier injection into the silicon layer **401**. The silicon layer **401** has an appropriate thickness, e.g., 70 nm or below. A surface of the silicon layer **401** of the SOI wafer **400** is first cleaned and then doped with the appropriate doping type (e.g., a p-type diode being doped by a p-type dopant such as boron, and a n-type diode being doped by a n-type dopant such as phosphorus), concentration (e.g., degenerate doping to minimize surface resistivity), and depth using an appropriate method (e.g., implantation, spin-on, or gas phase diffusion).

[0029] FIG. **5** depicts a graph **500** showing examples of current density versus voltage (J-V) characteristics for a MSM diode **506** with surface doping at a carrier injection side of a semiconductor layer and a MSM diode **508** without surface doping at a carrier injection side of a semiconductor layer. Graphic **500** includes axis **502**, axis **504**, curve **510**, and curve **512**. Axis **502** is the current density in amperes per cm^2. Axis **504** is the bias voltage in volts. Curve **510** depicts the current density versus voltage (J-V) characteristic for the MSM diode **506**. Curve **512** depicts the current density versus voltage (J-V) characteristic for the MSM diode **508**.

[0030] Each MSM diode **506** and **508** of FIG. **5** may be a p-type MSM diode having a cobalt (Co) layer M1, a silicon layer, and a platinum (Pt) layer M2. While the series resistance in a MSM diode is very low and is not a major current-limiting or speed-limiting component, the contact impedance R_C could become a rate-limiting factor when the diode is under a high forward bias (e.g., higher than flat-band bias). As shown in FIG. **5**, a current of the MSM diode **508** without surface doping deviates from the exponential curve **510** at approximately 0.2 V, the flat-band bias **520**, while a current of the MSM diode **506** with surface doping rises exponentially beyond the flat-band bias **520**. Depending on specific application and operating conditions, a MSM diode may contain a semiconductor layer with a doped surface or an undoped surface.

[0031] 2. Flip-Bond Fabrication

[0032] Returning to FIG. **4**, the surface-doped SOI wafer **400** is patterned by standard photolithography. The patterned photoresist may be crosslinked to enhance its resistance. The SOI wafer **400** is then etched (e.g., in O_2 plasma) to remove any photoresist residue in the patterned areas. Any newly formed silicon dioxide in the patterned areas is removed, for example, by briefly dipping the SOI wafer **400** in buffered oxide etch (BOE).

[0033] The SOI wafer **400** is loaded into a metal deposition (e.g., electron beam evaporation or sputter) chamber. When a base pressure of the chamber is sufficiently low (e.g., less than 2×10^{-6} Torr), a first metal **404**, such as platinum (Pt), is deposited (stage (b)). The Pt layer **404** has a thickness that is sufficiently large (e.g., 15 nm) to form excellent contact with the Si layer **401**. An aluminum (Al) layer (not shown) having a thickness that is sufficient for external connection or measurement contact (e.g., 100 nm) may be deposited on the Pt layer **404** at an appropriate rate (e.g., approximately 0.1 nm/sec) to ensure excellent metal film quality. Other metal materials different than Pt and Al may be used.

[0034] Following deposition of the metal layer **404**, the SOI wafer **400** is flipped and bonded onto a carrier wafer **405** using an adhesive **406** (stage (c)). The metal layer **404** is positioned between the Si layer **401** and the carrier wafer **405**. The adhesive **406** may be an insulating adhesive or a conducting adhesive. For example, a conducting adhesive may be used for bonding the SOI wafer **400** to the carrier wafer **405** when the surface-doped SOI wafer **400** is not patterned, e.g., when Pt and Al are directly deposited onto the surface-doped SOI wafer **400** as a uniform metal film without patterning.

[0035] At stage (d), the bulk silicon substrate **403** of the SOI wafer **400** is thinned down (e.g., by grinding or polishing using sandpaper) and completely removed by selective Si etching (e.g., using xenon difluoride (XeF_2) etch) to expose the SiO_2 layer **402**. At stage (e), the SiO_2 layer **402** is selectively etched away (e.g., by dipping in BOE). The remaining structure **407** is the thin device silicon layer **401** with the doped side and the previously deposited metal contact and electrode **404** bonded to the carrier wafer **405** by the adhesive **406**.

[0036] A second photolithography is performed to define second metal contact areas with designated registry to the Pt layer **404** on the other side of the device silicon layer **401**. The patterned photoresist may be crosslinked to enhance its resistance to the etching. The structure **407** is then etched (e.g., in O_2 plasma) to remove any photoresist residue in the patterned areas. Any newly formed silicon dioxide in the patterned areas is removed, for example, by briefly dipping in buffered oxide etch (BOE).

[0037] The structure **407** is loaded into a metal deposition (e.g., electron beam evaporation or sputter) chamber. When the base pressure of the chamber is sufficiently low (e.g., less than 2×10^{-6} Torr), a second metal, e.g., cobalt (Co), layer **408** is deposited (stage (f)). The Co layer **408** has a thickness that is sufficiently large (e.g., 15 nm) to form excellent contact with the Si layer **401**. An aluminum (Al) layer (not shown) having a thickness that is sufficient for external connection or measurement contact (e.g., 100 nm) may be deposited on the Co layer **408** at an appropriate rate (e.g., approximately 0.1 nm/sec) to ensure excellent metal film quality. Other metal materials different than Co and Al may be used. After the second metal layer **408** is deposited, the p-type Co—Si—Pt diodes **410** and **412** are ready for any electrical measurement or application.

[0038] The photolithography described above can be replaced by using shadow masks during the metal deposition. In general, any appropriate lithographic technique, including photolithography, electron-beam lithography, and imprint lithography, can also be applied. For example, electron beam lithography can be performed as an alternative to photolithography for smaller device sizes.

[0039] FIG. **6** depicts a graphs **600** and **650** showing examples of current density versus voltage (J-V) characteristics for different MSM diodes and a Schottky diode. Graphs **600** include axis **602**, axis **604**, and curves **610**, **612**, **614**, and **616**. Axis **602** is the current density in amperes per cm^2. Axis **604** is the bias voltage in volts. Curve **610** depicts a predicted semi-log J-V curve of a p-type iridium-silicon-iridium (Ir—Si—Ir) diode. Curve **612** depicts an experimental semi-log J-V curve of a p-type Co—Si—Pt diode. Curve **614** depicts an experimental semi-log J-V curve of a n-type chromium-silicon-chromium (Cr—Si—Cr) diode. Curve **616** depicts a theoretical semi-log J-V curve of a Cr—Si Schottky diode. For comparison, FIG. **6** includes a calculated J-V curve **616** for a standard Cr—Si Schottky diode and a predicted J-V curve **610** for a p-type Ir—Si—Ir MSM diode. Experimental